REMARKS

This amendment responds to the Office Action mailed April 23, 2002. Filed concurrently herewith is a *Request for a Two Month Extension of Time* which extends the shortened statutory period for response to expire on September 23, 2002. Accordingly, applicant respectfully submits that this response is being timely filed.

Claims 1-11 were pending. In this submission, claims 1 and 10 have been amended to more clearly define protection to which Applicants are entitled, and new claims 49 is submitted for examination on its merits. Thus, claims 1-11 and 49 are now pending in the present application and, for the reasons set forth below, are believed to be in condition for allowance.

SUMMARY OF THE INVENTION

The present invention is directed to a processor for executing instructions in units that are unrelated to the units in which the instructions are read from a program. The processor reads instructions from memory according to a first program counter which indicates a storage position of a processing packet in the memory. The processing packet has a size which is an integer number of bytes, and the storage position corresponds to a byte boundary. A second program counter is provided which indicates a position of a processing target instruction within the processing packet read from memory, where the processing target instruction position does not correspond to a byte boundary. As a result, the instructions to be executed can be freely set regardless of the amount of data read from memory. This allows instructions whose word length is not an integer number of bytes to be executed even when processing packets are read from memory in units of an integer number of bytes.

FORMALITIES

The Office Action rejected Claims 10-11 under 35 U.S.C. § 112, second paragraph, as being indefinite in that the functionality of these claims was unclear. By the above amendment, Claim 10 has been amended to more particularly point out and distinctly claim the subject matter of the present invention. Reconsideration is respectfully requested.

It was further requested in the Office Action that the functionality of Claims 10-11 be described. Claim 10 is directed to a first program counter for expressing the memory address of an instruction. The Examiner's attention is directed to page 35, lines 16-27 of the present specification where the functionality of expressing instruction addresses in accordance with amended Claim 10 is described as follows:

> Method for Expressing Instruction Addresses
>
> The following explains the method used to express instruction addresses in the present embodiment. Here, an instruction address refers to the address used to specify the position of a unit and is expressed as 32 bits.
>
> The upper 29-bits of a 32-bit address are used to specify an instruction packet and so are called the "packet address". This packet address is expressed as a 29-bit hexadecimal figure in a format such as "29'h012345467". A value produced by shifting the value of this packet address by 3-bits to the left is the memory address at which the instruction is stored.

PRIOR ART REJECTIONS

The Official Action rejected Claims 1-11 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,559,975 to *Christie et al.* This rejection is respectfully traversed in view of the above amendments, and reconsideration is requested based on the following remarks.

Independent Claim 1 recites a processor for reading instructions from memory according to a program counter and for executing the read instruction. Instructions are executed in units that are unrelated to the units in which the instructions are read from a program. In order to accomplish this feature, the program counter includes a first program counter which indicates a storage position of a processing packet in the memory. Claim 1 recites that the processing packet has a size which is an integer number of bytes, where the storage position is a position corresponding to a byte boundary.

The program counter further includes a second program counter which indicates a position of a processing target instruction within the processing packet read from memory, where amended Claim 1 recites that the position of which **does not correspond to a byte boundary**. By utilizing a position of the processing target instruction as not being a byte boundary, this allows instructions whose word length is not an integer number of bytes to be executed even when processing packets are read from memory in units of an integer number of bytes, and enables the processor to execute instructions which are not byte-aligned.

Christie Fails to Teach or Suggest a Program Counter which Indicates an Instruction Position which is Not at a Byte Boundary

Christie discloses a program counter update mechanism having a program counter having a 'less significant program counter portion' and a 'more significant program counter portion.' The 'less significant program counter portion' provides "less significant value bits" which indicate a position of a processing target instruction based on a selected one of a plurality of "less significant value bits" that are received, see col. 10, lines 42-65 and col. 18, lines 4-23. The 'more significant program counter portion' includes an incrementor to increment the present program counter value to the next instruction. As discussed in the Office Action, the 'less significant program counter portion' and the 'more significant program counter

portion' include adders, multiplexers, and other operators. The 'less significant value bits' are produced by addition or other general binary operation for providing the lower order bits of a memory address.

The Office Action asserts that the second program counter of Claim 1 is taught by the multiplexer of *Christie* which provides the least significant four bits of a potential next decode program counter value, where each potential next decode program counter value corresponds to a ROP from the queue. Applicants note that Claim 1 recites that the position of the processing target instruction **does not correspond to a byte boundary**. This feature is neither taught nor suggested by the teachings of *Christie*. To the contrary, *Christie* teaches in column 16, line 7-10 the following:

> Instruction decoder 108 maintains a decode program counter value for the ROP or ROPs corresponding to each of the x86 instructions in the byte queue 106 **by counting the number of bytes between instruction boundaries** or ... (emphasis added)

As can be seen from the foregoing, *Christie* explicitly states that the decode program counter value for each of the instructions is determined by counting the number of bytes between instruction boundaries. This requires that the position of the instruction of *Christie* to correspond to a byte boundary. Further, there is no description within *Christie* stating that the program counter is capable of indicating a position of the ROP regardless of whether the position corresponds to the byte boundary.

As set forth above, Claim 1 recites that the position of the processing target instruction indicated by the second program counter does not correspond to a byte boundary. *Christie* clearly fails to teach or suggest this feature, and Applicants respectfully submit that *Christie* neither anticipates nor renders obvious Claim 1 and its respective dependent claims 2-11. Reconsideration is respectfully requested.

Applicants further submit that the amendments to Claim 1 do not raise new issues requiring further search and/or consideration. It was discussed in detail of Applicant's last response filed on January 7, 2002 that the program counter of Claim 1 does not require a processing target instruction to correspond to a byte boundary (page 5, lines 22-23 of Applicants' last response) and that the program counter of *Christie* is not capable of indicating a position of a processing target instruction that is not a byte boundary (page 6, lines 16-18 of Applicants' last response). It is further recognized on page 3 of the most recent Office Action in discussing Applicants' previous arguments that the Examiner considered whether *Christie*'s less significant program counter teaches the feature of Applicant's second program counter, namely whether the processing target instruction position does not correspond to a byte boundary. Thus, Applicants respectfully submit that the subject matter of amended Claim 1 does not raise any new issues requiring further search and/or consideration.

Furthermore, new Claim 49 is submitted for examination on the merits which further stresses the feature of the second program counter of the processor of the present invention indicates a position of a processing target instruction which does not correspond to a byte boundary. The second program counter of Claim 49 further recites that the position of the processing target instruction is indicated by cycling through m different values, with m not being a power of 2, and sending a carry if the second program counter cycles. The concept of the second program counter cycling was previously examined with respect to Claim 2. Applicants respectfully submit that independent Claim 49 is separately patentable over the cited prior art of record.

INFORMATION DISCLOSURE STATEMENT

An IDS was filed on August 10, 1999 submitting Japanese Laid-Open Patent Application No. 62-42237 to the U.S. Patent Office along with a partial English translation of this reference. Applicants listed this document in the Information Disclosure Statement indicating that only a partial English translation

of the reference was submitted in compliance with 37 C.F.R. § 1.98(a)(1) and provided a copy of the partial translation in compliance with 37 CFR § 1.98(a)(3)(ii), which recites:

> A copy of the translation if a written English-language translation of a non-English-language document, or portion thereof, is within the possession, custody, or control of, or is readily available to any individual designated in § 1.56 (c).

Applicants submit that all of the necessary requirements were met at this time. However, this reference was not considered by the Examiner, since the form PTO 1449 submitted with the IDS did not indicate that a partial translation was submitted. Applicants note that use of a form PTO 1449 is not required, but is merely recommended in order to provide a "uniform listing of citations and with a ready way to indicate that the information has been considered," see MPEP § 609. Applicants original IDS complied with the requirements of 37 CFR § 1.98(a) by listing the document in the IDS (aside from the form PTO 1449) and also providing the partial translation of the document that was available. The Examiner appeared to believe the form PTO 1449 was misleading for not indicating that only a partial translation was considered by the Examiner.

In order to comply with the request of the Examiner in the previous Office Action, Applicants filed a revised form PTO 1449 on January 7, 2002 indicating that only a "partial" translation of the Japanese reference has been submitted. In the most recent Office Action, the Examiner has again refused to consider the Japanese reference since there the form PTO 1449 did not contain the word "Abstract." Applicants respectfully traverse this assertion and request proper consideration of the submitted Japanese reference.

Applicants initially note that there is no requirement in 37 CFR § 1.98 or in MPEP § 609 for the word "Abstract" to be written on a form PTO 1449. 37 CFR § 1.98(a) merely requires that the **portion of the English language translation**

available to the Applicants be submitted. Applicants complied with this requirement as well as the listing requirement by listing the Japanese reference properly in the original IDS along with a notation (**with partial English translation**), see the IDS filed on August 10, 1999, as well as in the form PTO 1449 filed on January 7, 2002. Furthermore, Applicants note that the partial English translation which was submitted was in fact the **English language Abstract** of the reference, which satisfies the requirement for the concise explanation of the relevance for non-English language information submitted, see M.P.E.P. § 609 (page 600-122, col. 2, 1st full paragraph).

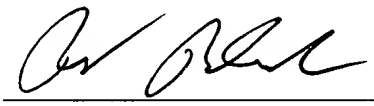
Through a careful and thorough review of M.P.E.P. § 609, Applicants cannot locate any requirement that the word "Abstract" appear on the list of references submitted. Applicants respectfully request that the provision within either the 37 CFR or the M.P.E.P be precisely identified which set forth this requirement asserted in the Office Action. Thus, Applicants respectfully submit that all of the requirements of 37 CFR § 1.97 and 1.98 were previously met by the prior information disclosure statements submitted and request consideration of this reference.

Notwithstanding the fact that all requirements have previously been satisfied, Applicants are merely submitting herewith a revised form PTO 1449 including the word "Abstract" to comply with the suggestions of the Examiner.

Applicant respectfully submits that all pending rejections have been overcome and Claims 1-11 and 49 are in proper condition for allowance. Early issuance of a Notice of Allowance is earnestly solicited. If a telephone or further personal conference would be helpful, the Examiner is invited to call the undersigned, who will cooperate in any appropriate manner to advance prosecution.

Respectfully Submitted,

PRICE AND GESS



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

New claim 49 has been submitted.

The claims have been amended as follows:

1. (Twice Amended) A processor for reading instructions from a memory according to a program counter, and for executing the read instruction,

the program counter including a first program counter and a second program counter,

the first program counter indicating a storage position of a processing packet in the memory, the processing packet being made of an integer number of bytes, the storage position being a position corresponding to a byte boundary,

the second program counter indicating a position of processing target instruction in the processing packet [regardless of whether the position corresponds to a byte boundary], the processing target instruction being an operation to be executed by the processor, and the position of which does not correspond to a byte boundary.

10. (Amended) The processor of Claim 1,

wherein the first program counter indicates bits of a memory address more significant than a $1 + log_2 n^{th}$ bit from a least significant, the memory address [being a] specifying the storage position [in the memory] of [a] the processing packet in memory [that is given by bit shifting the value in the first program counter by $log_2 n$ bits in a leftward direction], and n being a length of a processing packet in bytes.